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10/082,434	02/22/2002	Eliel Louzoun	42390P13579	6361

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EXAMINER	
TRUONG, BAO Q	
ART UNIT	PAPER NUMBER
2187	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/082,434	Applicant(s) LOUZOUN ET AL.	
	Examiner Bao Q Truong	Art Unit 2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-33 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-33 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 February 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The examiner acknowledges the applicant's submission of the amendment dated on 08 March 2004. At this point, claims 1, 7, 14, 22, and 28 have been amended. Thus, claims 1-33 are pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al. (U.S. Patent No. 6,453,370) in view of Stronging et al. (U.S. Patent No. 6,510,497 B1).

Referring to claim 1, Stracovsky teaches a method comprising:

receiving a plurality of commands to access at least one of a plurality of memory banks of a memory as receiving commands to access one of a plurality of memory banks from different requesting devices (see figures 1 and 8; and column 9: lines 30-36); and

scheduling the plurality of commands based at least in part on a status information of at least one of the plurality of memory banks as determining the sequence of operations to perform required request of resource based upon the determined status of the memory bank (see figures 3A-B and 4; Abstract; column 3: lines 15-20; and column 9: lines 40-52).

However, Stracovsky does not clearly teach a step of arbitrating between the commands to determine priority of access to the memory bus based at least in part on the status information.

Stronging teaches a method for scheduling memory access requests based on memory status (see Abstract). Furthermore, Stronging teaches a step of arbitrating between the requests to determine priority of access to the memory bus based at least in part on the status information of the memory (see column 17: lines 4-13).

It would have been obvious to one having an ordinary level of skill in the art at the time the invention was made to include, in the method taught by Stracovsky, a step of arbitrating between the commands to determine priority of access to the memory bus based at least in part on the status information. This would have been obvious because Stronging clearly teaches that arbitrating between the requests to determine priority of access to the memory bus based at least in part on the status information of the memory provides significant reductions in main memory latency (see column 8: lines 35-46; and column 12: lines 45-54).

As to claim 2, Stracovsky further teaches that the memory is a synchronous dynamic random access memory (see column 6: lines 36-42).

As to claim 3, Stracovsky further teaches that the status information is based at least in part on an idle state of the plurality of memory banks with respect to a bank based queuing scheme as having a determining if a memory bank is closed or opened by using information from bank register (see figure 8, column 11: lines 58-67, and column 12: table 2).

As to claim 4, Stracovsky further teaches that the status information is an idle state of the plurality of memory banks as a memory bank is closed or opened (see column 11: lines 58-67, and column 12: table 2).

As to claim 5, Stracovsky further teaches that the status information is based at least in part on a type of a most recent command forwarded to the memory device via a memory bus (see figure 3B, column 7: lines 40-53).

As to claim 6, Stracovsky further teaches that the plurality of commands are read and write commands (see column 6: lines 2-4, column 9: lines 30-36).

Referring to claim 7, Stracovsky discloses a system comprising:

a processor (see figures 1A-D: element 102); and

a logic as a device controller (see figure 1A-D and 8: element 104), coupled to the processor and to at least one memory device with a plurality of memory banks (see figure 8: element 704), to receive commands to access the memory device as receiving commands to access one of a plurality of memory banks from different requesting devices (see figures 1 and 8; and column 9: lines 30-36) and to schedule the commands based at least in part on a status information of the plurality of memory banks as determining the sequence of operations to perform required request of resource based upon the determined status of the memory bank (see figures 3A-B and 4; Abstract; column 3: lines 15-20; and column 9: lines 40-52).

However, Stracovsky does not clearly disclose the device controller arbitrating the commands based at least in part on the status information of the plurality of memory banks.

Stronging discloses a system for scheduling memory access requests based on memory status (see Abstract). Furthermore, Stronging discloses a memory arbiter (see figure 4: element 482; and column 11: lines 21-27) arbitrating the commands based at least in part on the status information of the plurality of memory banks (see column 17: lines 4-13).

It would have been obvious to one having an ordinary level of skill in the art at the time the invention was made to modify the device controller disclosed by Stracovsky to arbitrate the commands based at least in part on the status information of the plurality of memory banks. This would have been obvious because Stronging clearly teaches that arbitrating between the requests to determine priority of access to the memory bus based at least in part on the status information of the memory provides significant reductions in main memory latency (see column 8: lines 35-46; and column 12: lines 45-54).

As to claim 8, Stracovsky further discloses that the commands are read and write commands (see column 6: lines 2-4, column 9: lines 30-36).

As to claim 9, Stracovsky further discloses that the status information is based at least in part on a type of a most recent command forwarded to the memory device via a memory bus (see figure 3B, column 7: lines 40-53).

As to claim 10, Stracovsky further discloses that the plurality of memory banks perform in parallel as each bank has its bank register, bank number comparator, etc (see figure 8).

As to claim 11, Stracovsky further discloses that the logic is a network switch or a memory controller (see figure 1A-D and 8: element 104).

As to claim 12, Stracovsky further discloses that the status information is an idle state of the plurality of memory banks as a memory bank is closed or opened (see column 11: lines 58-67, and column 12: table 2).

As to claim 13, Stracovsky further discloses that the memory is a synchronous dynamic random access memory (see column 6: lines 36-42).

Referring to claim 14, Stracovsky discloses an apparatus comprising:

a first logic as a system interface (see figure 1B: element 110), coupled to at least one memory device with a plurality of memory banks (see figure 8: element 704), to received commands to access the memory devices (see column 6: lines 54-64); and

a second logic as a command sequencer (see figure 1B: element 116), coupled to the first logic, to schedule the received commands based at least in part on a status information of the plurality of memory banks as determining the sequence of operations to perform required request of resource based upon the determined status of the memory bank (see figures 3A-B and 4; Abstract; column 3: lines 15-20; and column 9: lines 40-52).

However, Stracovsky does not clearly disclose the command sequencer arbitrating the received commands based at least in part on the status information of the plurality of memory banks.

Stronging discloses a system for scheduling memory access requests based on memory status (see Abstract). Furthermore, Stronging discloses a memory arbiter (see figure 4: element 482; and column 11: lines 21-27) arbitrating the commands based at least in part on the status information of the plurality of memory banks (see column 17: lines 4-13).

It would have been obvious to one having an ordinary level of skill in the art at the time the invention was made to modify the command sequencer disclosed by Stracovsky to arbitrate the received commands based at least in part on the status information of the plurality of memory banks. This would have been obvious because Stronging clearly teaches that arbitrating between the requests to determine priority of access to the memory bus based at least in part on the status information of the memory provides significant reductions in main memory latency (see column 8: lines 35-46; and column 12: lines 45-54).

As to claim 15, Stracovsky further discloses that the apparatus comprises a third logic (see figure 8: element 800) to forward the schedule of the received commands to the memory device via a memory bus.

As to claim 16, Stracovsky further discloses that the apparatus is either one of a network switch or a memory controller (see figure 1A-D and 8: element 104).

As to claim 17, Stracovsky further discloses that the memory device is a synchronous dynamic random access memory (see column 6: lines 36-42).

As to claim 18, Stracovsky further discloses that the received commands are read and write commands (see column 6: lines 2-4, column 9: lines 30-36).

As to claim 19, Stracovsky further discloses that the status information is based at least in part on a type of a most recent command forwarded to the memory device via the memory bus (see figure 3B, column 7: lines 40-53).

As to claim 20, Stracovsky further discloses that the plurality of memory banks perform in parallel as each bank has its bank register, bank number comparator, etc (see figure 8).

As to claim 21, Stracovsky further discloses that the status information is an idle state of the plurality of memory banks as a memory bank is closed or opened (see column 11: lines 58-67, and column 12: table 2).

Referring to claim 22, Stracovsky teaches a method comprising:

receiving a plurality of commands to access at least one of a plurality of memory banks of a memory as receiving commands to access one of a plurality of memory banks from different requesting devices (see figures 1 and 8; and column 9: lines 30-36); and

scheduling the plurality of commands based at least in part on a status information of at least one of the plurality of memory banks as determining the sequence of operations to perform required request of resource based upon the determined status of the memory bank (see figures 3A-B and 4; Abstract; column 3: lines 15-20; and column 9: lines 40-52).

However, Stracovsky does not clearly teach a step of arbitrating between the commands to determine priority of access to the memory bus based at least in part on the status information.

Stronging teaches a method for scheduling memory access requests based on memory status (see Abstract). Furthermore, Stronging teaches a step of arbitrating between the requests to determine priority of access to the memory bus based at least in part on the status information of the memory (see column 17: lines 4-13).

It would have been obvious to one having an ordinary level of skill in the art at the time the invention was made to include, in the method taught by Stracovsky, a step of arbitrating between the commands to determine priority of access to the memory bus based at least in part on the status information. This would have been obvious because Stronging clearly teaches that arbitrating between the requests to determine priority of access to the memory bus based at least in part on the status information of the memory provides significant reductions in main memory latency (see column 8: lines 35-46; and column 12: lines 45-54).

As to claim 23, Stracovsky further teaches that the memory device is a synchronous dynamic random access memory (see column 6: lines 36-42).

As to claim 24, Stracovsky further teaches that the status information is an idle state of the plurality of memory banks as a memory bank is closed or opened (see column 11: lines 58-67, and column 12: table 2).

As to claim 25, Stracovsky further teaches that the plurality of memory banks perform in parallel as each bank has its bank register, bank number comparator, etc (see figure 8).

As to claim 26, Stracovsky further teaches that the status information is based at least in part on a type of a most recent command forwarded to the memory device via the memory bus (see figure 3B, column 7: lines 40-53).

As to claim 27, Stracovsky further teaches that the received commands are read and write commands (see column 6: lines 2-4, column 9: lines 30-36).

Referring to claim 28, Stracovsky and Stronging teach the method of claims 22 in a computer environment. Inherently, it can be embodied as instruction codes on a computer readable media and executed by a computing platform as in claim 28.

As to claim 29, Stracovsky further teaches that the memory is a synchronous dynamic random access memory (see column 6: lines 36-42).

As to claim 30, Stracovsky further teaches that the status information is an idle state of the plurality of memory banks as a memory bank is closed or opened (see column 11: lines 58-67, and column 12: table 2).

As to claim 31, Stracovsky further teaches that the plurality of memory banks perform in parallel as each bank has its bank register, bank number comparator, etc (see figure 8).

As to claim 32, Stracovsky further teaches that the status information is based at least in part on a type of a most recent command forwarded to the memory device via a memory bus (see figure 3B, column 7: lines 40-53).

As to claim 33, Stracovsky further teaches that the received commands are read and write commands (see column 6: lines 2-4, column 9: lines 30-36).

Response to Arguments

4. Applicant's arguments filed on 08 March 2004 have been fully considered but they are not persuasive.

Regarding the rejection of claim 22, the applicant argues on page 8-9 that Bass teaches away from the concept of claim 22. The examiner disagrees and directs the applicant to the original language of claim 22 (before being amended). Originally, claim 22 comprises a method step of "arbitrating between the commands to determine priority of access the memory bus". The arbitration is **not** based on the status information. Bass teaches a step of arbitrating requests for access to system resources using round robin method. Clearly, Bass teaches the above mentioned method step of claim 22.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **three months** from the mailing date of this action. In the event a first reply is filed within **two months** of the mailing date of this final action and the advisory action is not mailed until after the end of the **three-month** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **six months** from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bao Q Truong whose telephone number is (703) 308-7090. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

BAO QUOC TRUONG

BT

Patent Examiner

4 May 2004

Donald A. Sparks

Supervisory Patent Examiner

Technology Center 2100